PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Haruo NISHIDA et al. Group Art Unit: 2117

Application No.: 10/766,038 Examiner: J. KERVEROS

Filed: January 29, 2004 Docket No.: 118497

For: AN INTEGRATED TEST CIRCUIT, A TEST CIRCUIT, AND A TEST METHOD FOR PERFORMING TRANSMISSION AND RECEPTION PROCESSING TO AND FROM A FIRST AND A SECOND MACRO BLOCK AT A FIRST FREQUENCY (As amended)

AMENDMENT UNDER 37 C.F.R. §1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the April 24, 2007 Office Action, and in consideration of the July 23, 2007 personal interview with the Examiner, please consider the following:

Amendments to the Specification;

Amendments to the Claims as reflected in the listing of claims; and

Remarks.